

Features

- High Performance, Low Power AVR[®] 8-Bit Microcontroller
- Advanced RISC Architecture
 - 120 Powerful Instructions – Most Single Clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
- Non-volatile Program and Data Memories
 - 2/4/8K Byte of In-System Programmable Program Memory Flash (ATtiny25/45/85)
Endurance: 10,000 Write/Erase Cycles
 - 128/256/512 Bytes In-System Programmable EEPROM (ATtiny25/45/85)
Endurance: 100,000 Write/Erase Cycles
 - 128/256/512 Bytes Internal SRAM (ATtiny25/45/85)
 - Programming Lock for Self-Programming Flash Program and EEPROM Data Security
- Peripheral Features
 - 8-bit Timer/Counter with Prescaler and Two PWM Channels
 - 8-bit High Speed Timer/Counter with Separate Prescaler
2 High Frequency PWM Outputs with Separate Output Compare Registers
Programmable Dead Time Generator
 - USI – Universal Serial Interface with Start Condition Detector
 - 10-bit ADC
 - 4 Single Ended Channels
 - 2 Differential ADC Channel Pairs with Programmable Gain (1x, 20x)
Temperature Measurement
 - Programmable Watchdog Timer with Separate On-chip Oscillator
 - On-chip Analog Comparator
- Special Microcontroller Features
 - debugWIRE On-chip Debug System
 - In-System Programmable via SPI Port
 - External and Internal Interrupt Sources
 - Low Power Idle, ADC Noise Reduction, and Power-down Modes
 - Enhanced Power-on Reset Circuit
 - Programmable Brown-out Detection Circuit
 - Internal Calibrated Oscillator
- I/O and Packages
 - Six Programmable I/O Lines
 - 8-pin PDIP, 8-pin SOIC and 20-pad QFN/MLF
- Operating Voltage
 - 1.8 - 5.5V for ATtiny25/45/85V
 - 2.7 - 5.5V for ATtiny25/45/85
- Speed Grade
 - ATtiny25/45/85V: 0 - 4 MHz @ 1.8 - 5.5V, 0 - 10 MHz @ 2.7 - 5.5V
 - ATtiny25/45/85: 0 - 10 MHz @ 2.7 - 5.5V, 0 - 20 MHz @ 4.5 - 5.5V
- Industrial Temperature Range
- Low Power Consumption
 - Active Mode:
1 MHz, 1.8V: 300 μ A
 - Power-down Mode:
0.1 μ A at 1.8V



**8-bit AVR[®]
Microcontroller
with 2/4/8K
Bytes In-System
Programmable
Flash**

**ATtiny25/V*
ATtiny45/V
ATtiny85/V***

Summary

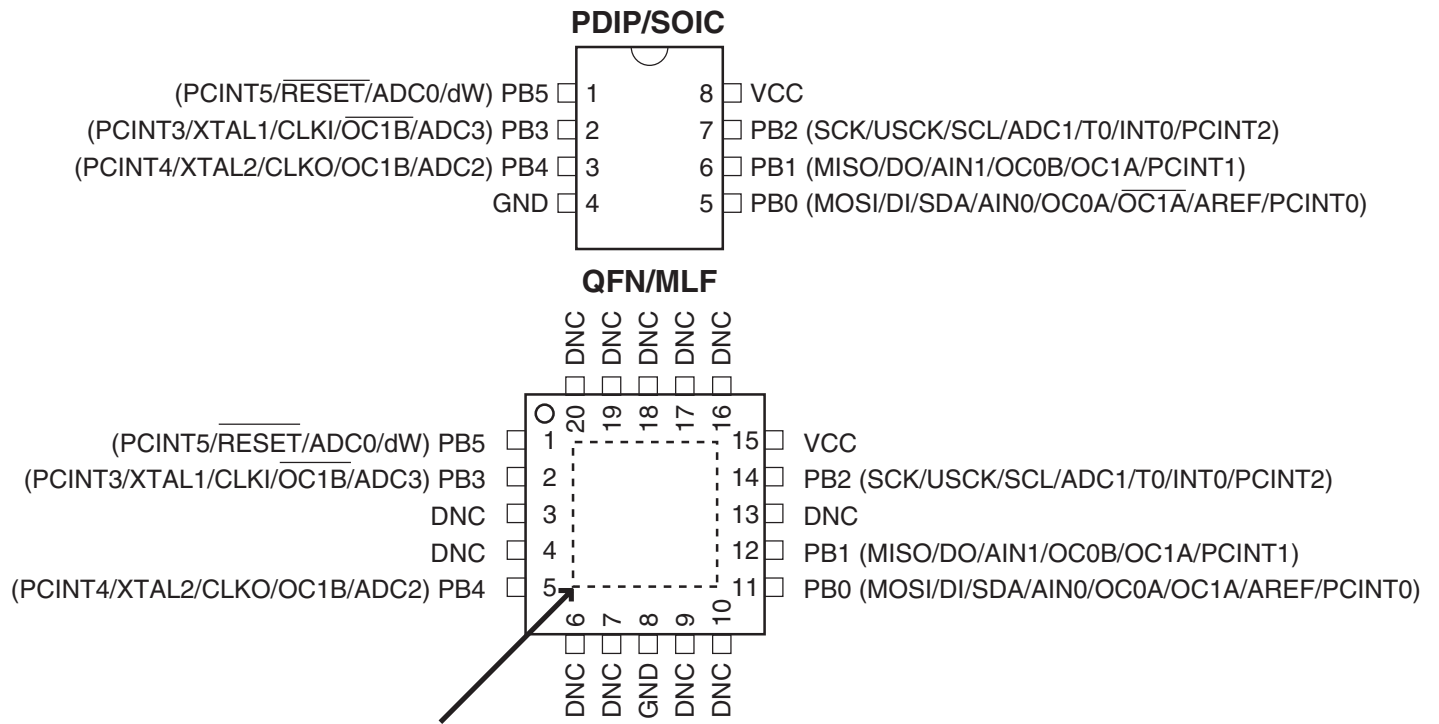
***Preliminary**

2586JS-AVR-12/06



1. Pin Configurations

Figure 1-1. Pinout ATtiny25/45/85



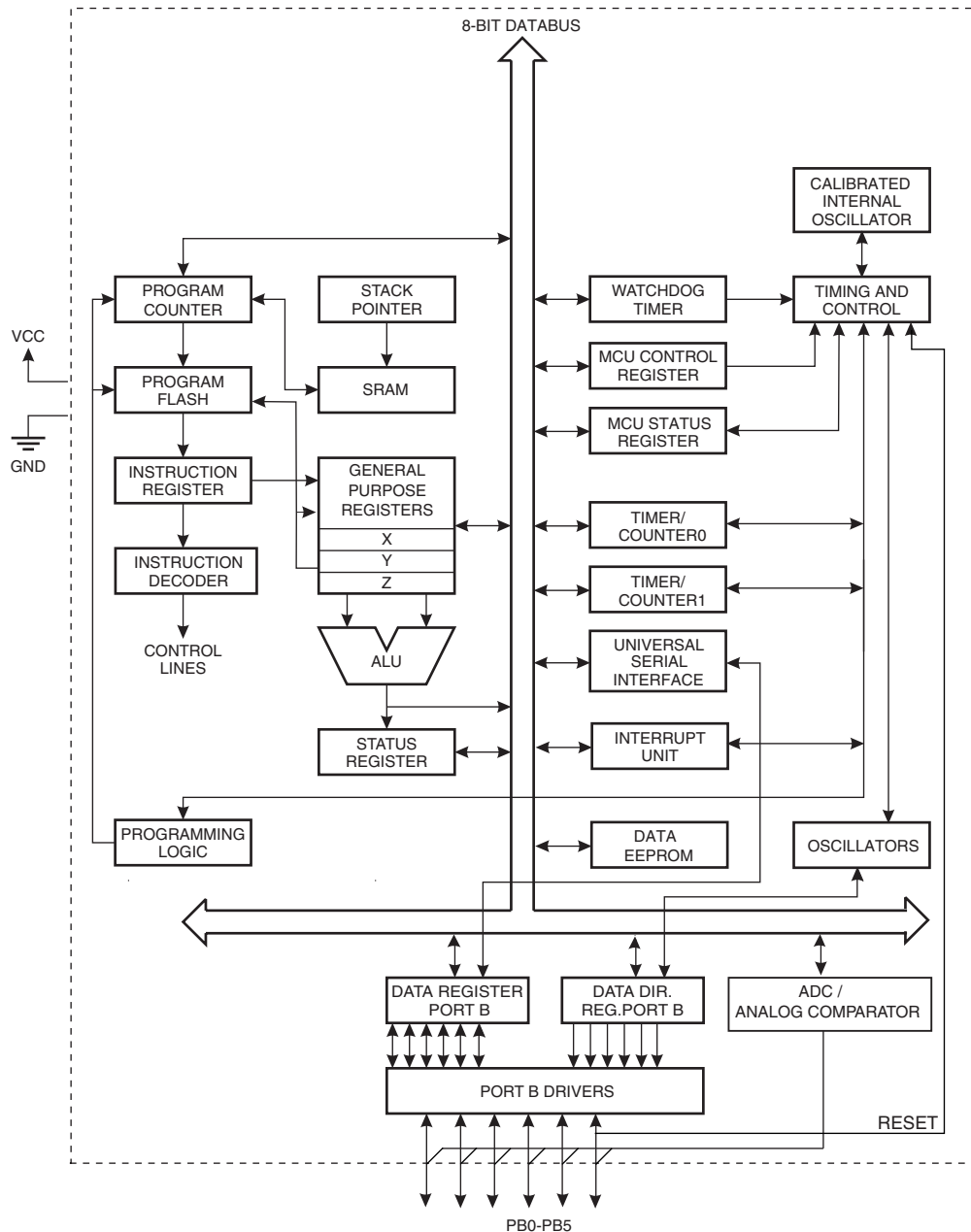
NOTE: Bottom pad should be soldered to ground.
DNC: Do Not Connect

2. Overview

The ATtiny25/45/85 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny25/45/85 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block Diagram

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent



registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny25/45/85 provides the following features: 2/4/8K byte of In-System Programmable Flash, 128/256/512 bytes EEPROM, 128/256/256 bytes SRAM, 6 general purpose I/O lines, 32 general purpose working registers, one 8-bit Timer/Counter with compare modes, one 8-bit high speed Timer/Counter, Universal Serial Interface, Internal and External Interrupts, a 4-channel, 10-bit ADC, a programmable Watchdog Timer with internal Oscillator, and three software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, Analog Comparator, and Interrupt system to continue functioning. The Power-down mode saves the register contents, disabling all chip functions until the next Interrupt or Hardware Reset. The ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the Program memory to be re-programmed In-System through an SPI serial interface, by a conventional non-volatile memory programmer or by an On-chip boot code running on the AVR core.

The ATtiny25/45/85 AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

2.2 Pin Descriptions

2.2.1 VCC

Supply voltage.

2.2.2 GND

Ground.

2.2.3 Port B (PB5..PB0)

Port B is a 6-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATtiny25/45/85 as listed on [page 61](#).

On the ATtiny25 device the programmable I/O ports PB3 and PB4 (pins 2 and 3) are exchanged in the ATtiny15 compatibility mode for supporting the backward compatibility with ATtiny15.

2.2.4 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in [Table 23-3 on page 170](#). Shorter pulses are not guaranteed to generate a reset.

3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on <http://www.atmel.com/avr>.



4. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x3F	SREG	I	T	H	S	V	N	Z	C	page 7
0x3E	SPH	–	–	–	–	–	–	SP9	SP8	page 10
0x3D	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	page 10
0x3C	Reserved	–	–	–	–	–	–	–	–	
0x3B	GIMSK	–	INT0	PCIE	–	–	–	–	–	page 51
0x3A	GIFR	–	INTF0	PCIF	–	–	–	–	–	page 52
0x39	TIMSK	–	OCIE1A	OCIE1B	OCIE0A	OCIE0B	TOIE1	TOIE0	–	page 84/page 106
0x38	TIFR	–	OCF1A	OCF1B	OCF0A	OCF0B	TOV1	TOV0	–	page 84
0x37	SPMCSR	–	–	–	CTPB	RFLB	PGWRT	PGERS	SPMEN	page 148
0x36	Reserved	–	–	–	–	–	–	–	–	
0x35	MCUCR	BODS	PUD	SE	SM1	SM0	BODSE	ISC01	ISC00	page 37, page 51, page 65,
0x34	MCUSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	page 44,
0x33	TCCR0B	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	page 82
0x32	TCNT0	Timer/Counter0								page 83
0x31	OSCCAL	Oscillator Calibration Register								page 31
0x30	TCCR1	CTC1	PWM1A	COM1A1	COM1A0	CS13	CS12	CS11	CS10	page 92, page 103
0x2F	TCNT1	Timer/Counter1								page 94, page 105
0x2E	OCR1A	Timer/Counter1 Output Compare Register A								page 94, page 105
0x2D	OCR1C	Timer/Counter1 Output Compare Register C								page 95, page 106
0x2C	GTCCR	TSM	PWM1B	COM1B1	COM1B0	FOC1B	FOC1A	PSR1	PSR0	page 79, page 93, page
0x2B	OCR1B	Timer/Counter1 Output Compare Register B								page 95
0x2A	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00	page 79
0x29	OCR0A	Timer/Counter0 – Output Compare Register A								page 83
0x28	OCR0B	Timer/Counter0 – Output Compare Register B								page 84
0x27	PLLCSR	LSM	–	–	–	–	PCKE	PLLE	PLOCK	page 97, page 107
0x26	CLKPR	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	page 32
0x25	DT1A	DT1AH3	DT1AH2	DT1AH1	DT1AH0	DT1AL3	DT1AL2	DT1AL1	DT1AL0	page 109
0x24	DT1B	DT1BH3	DT1BH2	DT1BH1	DT1BH0	DT1BL3	DT1BL2	DT1BL1	DT1BL0	page 110
0x23	DTPS1	–	–	–	–	–	–	DTPS11	DTPS10	page 109
0x22	DWDR	DWDR[7:0]								page 145
0x21	WDTCR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	page 44
0x20	PRR	–	–	–	–	PRTIM1	PRTIM0	PRUSI	PRADC	page 36
0x1F	EEARH	–	–	–	–	–	–	–	EEAR8	page 19
0x1E	EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	page 19
0x1D	EEDR	EEPROM Data Register								page 19
0x1C	EECR	–	–	EPM1	EPM0	EERIE	EEMPE	EEPE	EERE	page 20
0x1B	Reserved	–	–	–	–	–	–	–	–	
0x1A	Reserved	–	–	–	–	–	–	–	–	
0x19	Reserved	–	–	–	–	–	–	–	–	
0x18	PORTB	–	–	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	page 65
0x17	DDRB	–	–	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	page 65
0x16	PINB	–	–	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	page 65
0x15	PCMSK	–	–	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	page 52
0x14	DIDR0	–	–	ADC0D	ADC2D	ADC3D	ADC1D	AIN1D	AIN0D	page 125, page 143
0x13	GPOR2	General Purpose I/O Register 2								page 9
0x12	GPOR1	General Purpose I/O Register 1								page 9
0x11	GPOR0	General Purpose I/O Register 0								page 9
0x10	USIBR	USI Buffer Register								page 119
0x0F	USIDR	USI Data Register								page 118
0x0E	USISR	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	page 119
0x0D	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	page 120
0x0C	Reserved	–	–	–	–	–	–	–	–	
0x0B	Reserved	–	–	–	–	–	–	–	–	
0x0A	Reserved	–	–	–	–	–	–	–	–	
0x09	Reserved	–	–	–	–	–	–	–	–	
0x08	ACSR	ACD	ACBG	ACO	ACI	ACIE	–	ACIS1	ACIS0	page 124
0x07	ADMUX	REFS1	REFS0	ADLAR	REFS2	MUX3	MUX2	MUX1	MUX0	page 138
0x06	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	page 140
0x05	ADCH	ADC Data Register High Byte								page 141
0x04	ADCL	ADC Data Register Low Byte								page 141
0x03	ADCSRB	BIN	ACME	IPR	–	–	ADTS2	ADTS1	ADTS0	page 124, page 142
0x02	Reserved	–	–	–	–	–	–	–	–	
0x01	Reserved	–	–	–	–	–	–	–	–	
0x00	Reserved	–	–	–	–	–	–	–	–	

- Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
 3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVR, the CBI and SBI instructions will only operation the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

5. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rd,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	Rd,K	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \cdot Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \cdot K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow 0x00 - Rd$	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \cdot (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \cdot Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow 0xFF$	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	$PC \leftarrow STACK$	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) $PC \leftarrow PC + 2$ or 3	None	1/2/3
CP	Rd,Rr	Compare	$Rd - Rr$	Z, N, V, C, H	1
CPC	Rd,Rr	Compare with Carry	$Rd - Rr - C$	Z, N, V, C, H	1
CPI	Rd,K	Compare Register with Immediate	$Rd - K$	Z, N, V, C, H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N \oplus V = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N \oplus V = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	$I/O(P,b) \leftarrow 1$	None	2
CBI	P,b	Clear Bit in I/O Register	$I/O(P,b) \leftarrow 0$	None	2
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z,C,N,V	1

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=0..6$	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	$Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry	$C \leftarrow 0$	C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	$I \leftarrow 1$	I	1
CLI		Global Interrupt Disable	$I \leftarrow 0$	I	1
SES		Set Signed Test Flag	$S \leftarrow 1$	S	1
CLS		Clear Signed Test Flag	$S \leftarrow 0$	S	1
SEV		Set Twos Complement Overflow	$V \leftarrow 1$	V	1
CLV		Clear Twos Complement Overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	$T \leftarrow 1$	T	1
CLT		Clear T in SREG	$T \leftarrow 0$	T	1
SEH		Set Half Carry Flag in SREG	$H \leftarrow 1$	H	1
CLH		Clear Half Carry Flag in SREG	$H \leftarrow 0$	H	1
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	$Rd \leftarrow Rr$	None	1
MOVW	Rd, Rr	Copy Register Word	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, -X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2
LD	Rd, -Y	Load Indirect and Pre-Dec.	$Y \leftarrow Y - 1, Rd \leftarrow (Y)$	None	2
LDD	Rd, Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1, Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow Rr, X \leftarrow X + 1$	None	2
ST	-X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	-Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
STD	Y+q, Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2
ST	Z, Rr	Store Indirect	$(Z) \leftarrow Rr$	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None	2
STD	Z+q, Rr	Store Indirect with Displacement	$(Z + q) \leftarrow Rr$	None	2
STS	k, Rr	Store Direct to SRAM	$(k) \leftarrow Rr$	None	2
LPM		Load Program Memory	$R0 \leftarrow (Z)$	None	3
LPM	Rd, Z	Load Program Memory	$Rd \leftarrow (Z)$	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	3
SPM		Store Program Memory	$(z) \leftarrow R1:R0$	None	
IN	Rd, P	In Port	$Rd \leftarrow P$	None	1
OUT	P, Rr	Out Port	$P \leftarrow Rr$	None	1
PUSH	Rr	Push Register on Stack	$STACK \leftarrow Rr$	None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/Timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A



6. Ordering Information

6.1 ATtiny25

Speed (MHz) ⁽³⁾	Power Supply	Ordering Code ⁽²⁾	Package ⁽¹⁾	Operational Range
10	1.8 - 5.5V	ATtiny25V-10PU ATtiny25V-10SU ATtiny25V-10MU	8P3 8S2 20M1	Industrial (-40°C to 85°C)
20	2.7 - 5.5V	ATtiny25-20PU ATtiny25-20SU ATtiny25-20MU	8P3 8S2 20M1	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} , see [Figure 23.3 on page 168](#)

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-lead, 0.209" Wide, Plastic Gull-Wing Small Outline (EIAJ SOIC)
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

6.2 ATtiny45

Speed (MHz) ⁽³⁾	Power Supply	Ordering Code ⁽²⁾	Package ⁽¹⁾	Operational Range
10	1.8 - 5.5V	ATtiny45V-10PU ATtiny45V-10SU ATtiny45V-10MU	8P3 8S2 20M1	Industrial (-40°C to 85°C)
20	2.7 - 5.5V	ATtiny45-20PU ATtiny45-20SU ATtiny45-20MU	8P3 8S2 20M1	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} , see [Figure 23.3 on page 168](#)

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-lead, 0.209" Wide, Plastic Gull-Wing Small Outline (EIAJ SOIC)
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

6.3 ATtiny85

Speed (MHz) ⁽³⁾	Power Supply	Ordering Code ⁽²⁾	Package ⁽¹⁾	Operational Range
10	1.8 - 5.5V	ATtiny85V-10PU ATtiny85V-10SU ATtiny85V-10MU	8P3 8S2 20M1	Industrial (-40°C to 85°C)
20	2.7 - 5.5V	ATtiny85-20PU ATtiny85-20SU ATtiny85-20MU	8P3 8S2 20M1	Industrial (-40°C to 85°C)

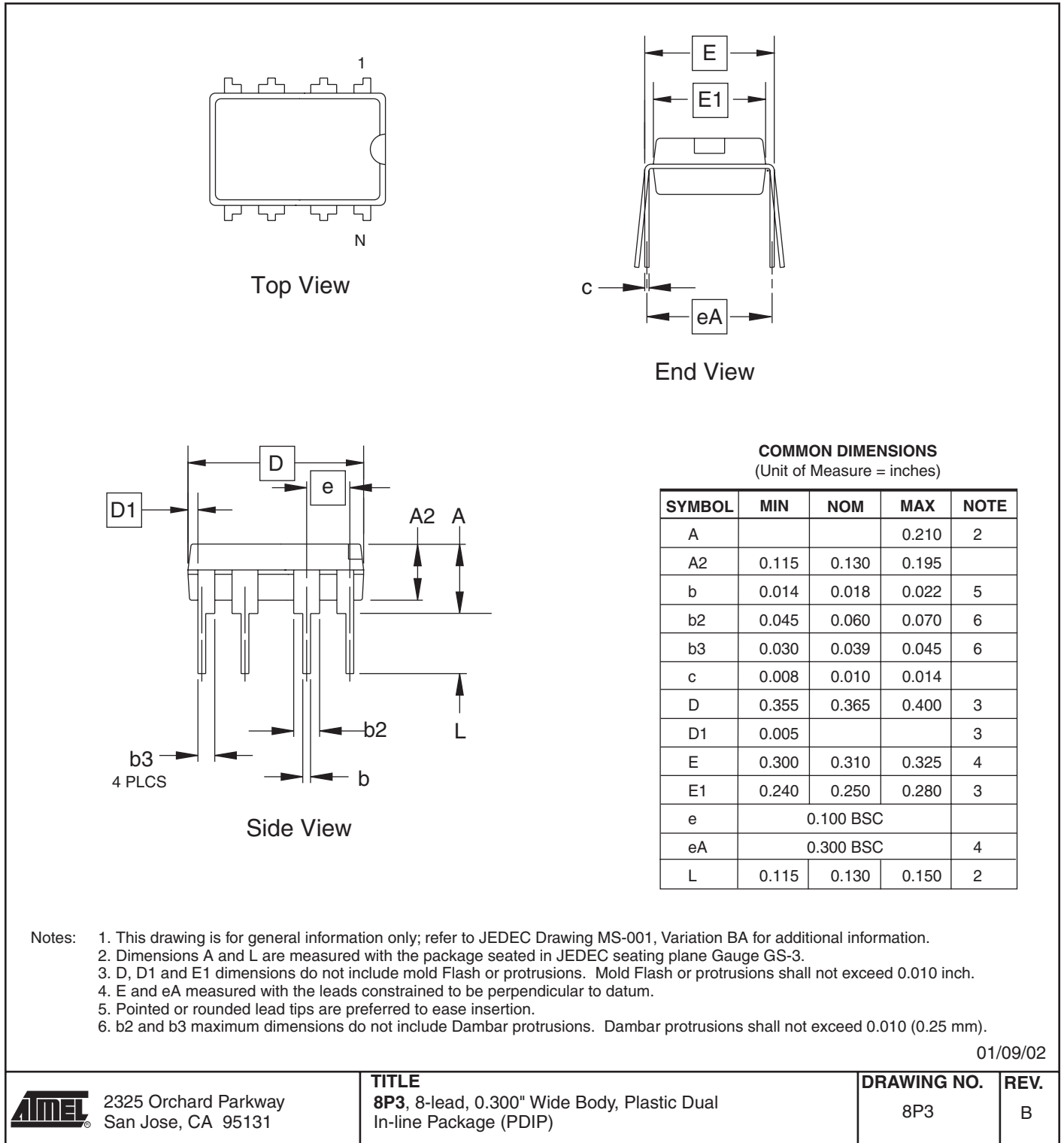
- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} , see [Figure 23.3 on page 168](#)

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-lead, 0.209" Wide, Plastic Gull-Wing Small Outline (EIAJ SOIC)
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

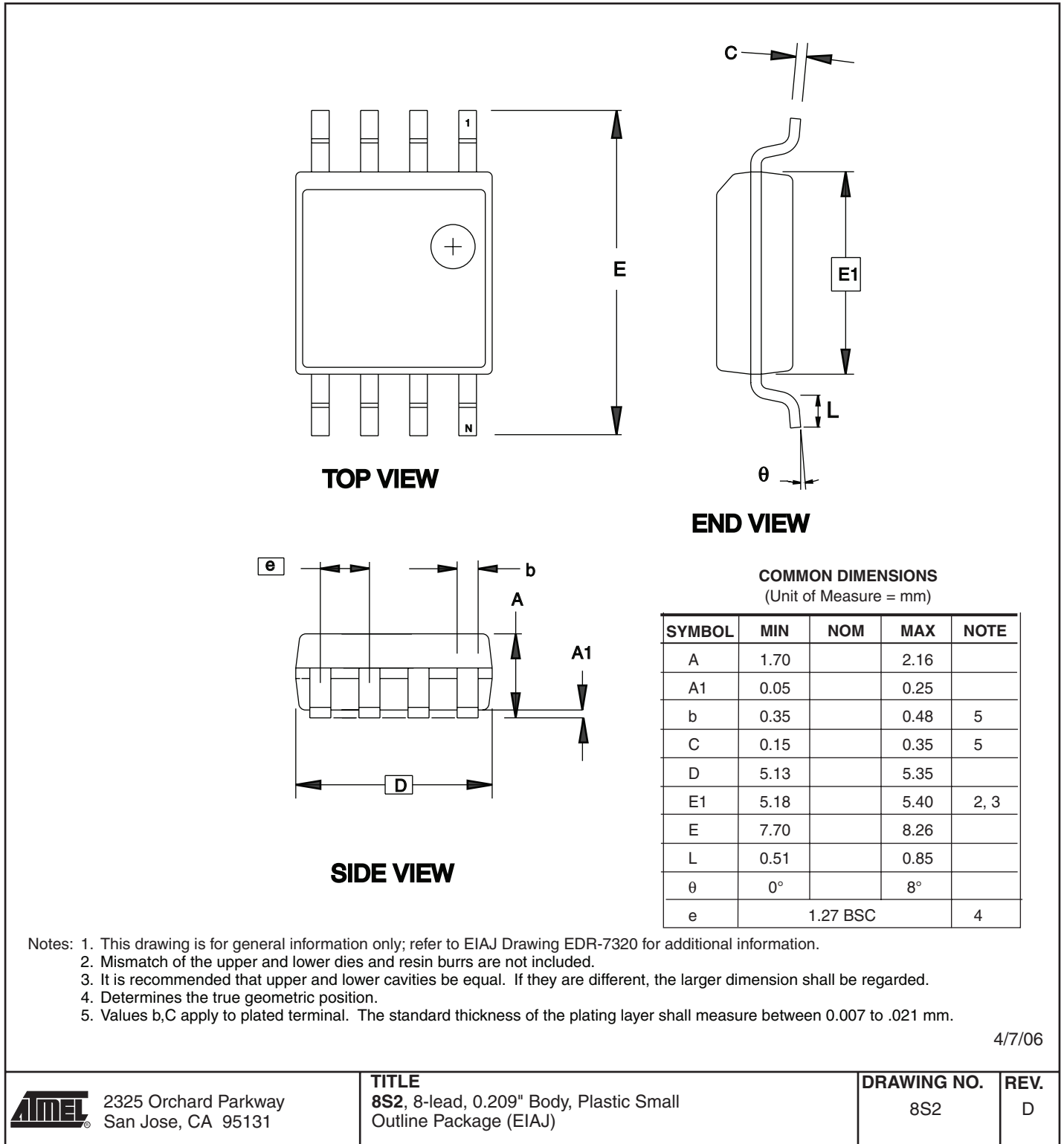
12 ATtiny25/45/85

7. Packaging Information

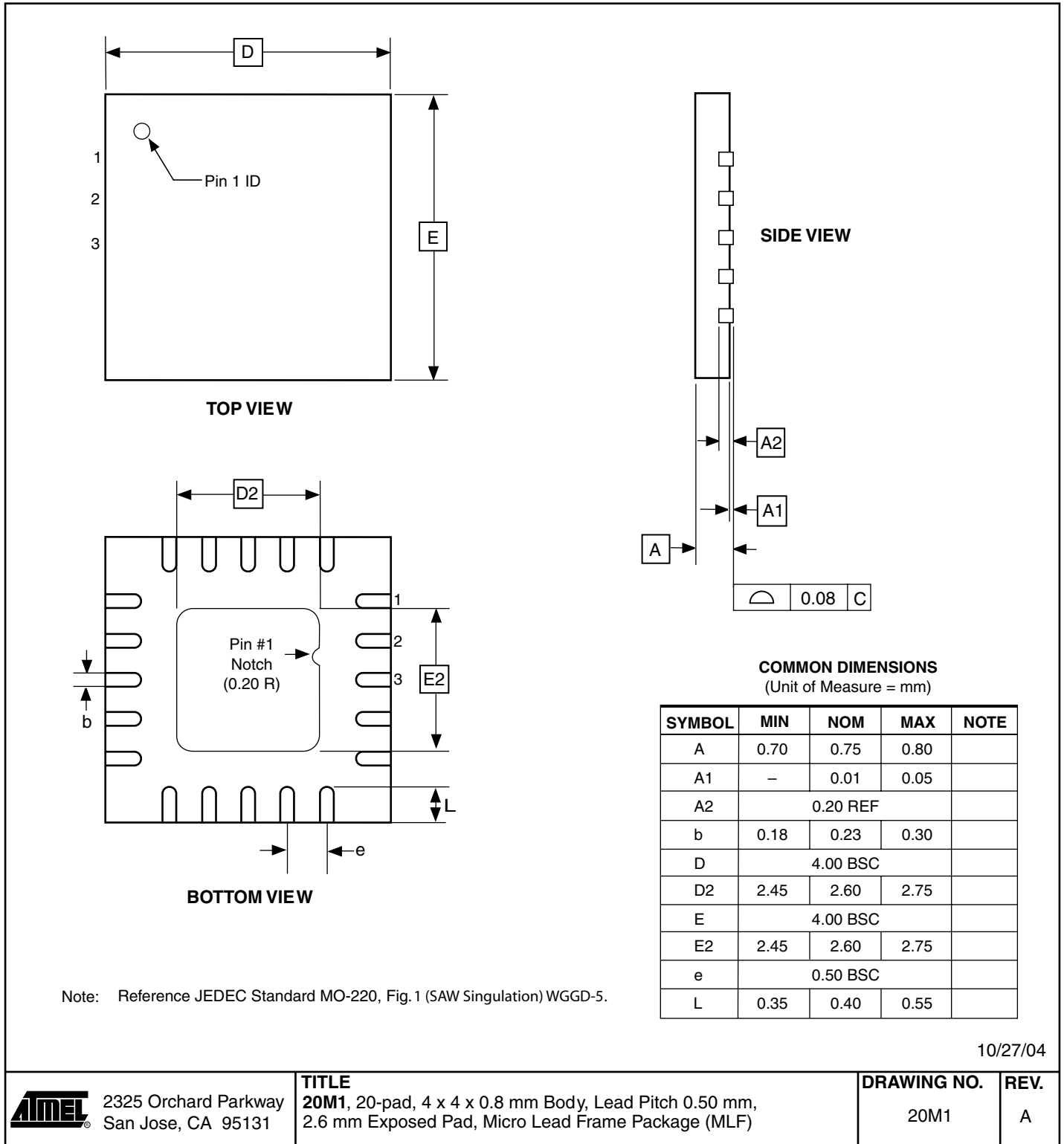
7.1 8P3



7.2 8S2



7.3 20M1



8. Errata

8.1 Errata ATtiny25

The revision letter in this section refers to the revision of the ATtiny25 device.

8.1.1 Rev C

No known errata

8.1.2 Rev B

- **Reading EEPROM at low frequency may not work for frequencies below 900 kHz**

1. **Reading EEPROM at low frequency may not work for frequencies below 900 kHz**

Reading data from the EEPROM at low internal clock frequency may result in wrong data read.

Problem Fix/Workaround

Avoid using the EEPROM at clock frequency below 900kHz.

8.1.3 Rev A

Not sampled.

8.2 Errata ATtiny45

The revision letter in this section refers to the revision of the ATtiny45 device.

8.2.1 Rev E

No known errata

8.2.2 Rev D

- **Reading EEPROM at low frequency may not work for frequencies below 900 kHz**

1. **Reading EEPROM at low frequency may not work for frequencies below 900 kHz**

Reading data from the EEPROM at low internal clock frequency may result in wrong data read.

Problem Fix/Workaround

Avoid using the EEPROM at clock frequency below 900kHz.

8.2.3 Rev B and C

- **PLL not locking**
- **EEPROM read from application code does not work in Lock Bit Mode 3**
- **Reading EEPROM at low frequency may not work for frequencies below 900 kHz**
- **Timer Counter 1 PWM output generation on OC1B- XOC1B does not work correctly**

1. **PLL not locking**

When at frequencies below 6.0 MHz, the PLL will not lock

Problem fix / Workaround

When using the PLL, run at 6.0 MHz or higher.

2. **EEPROM read from application code does not work in Lock Bit Mode 3**

When the Memory Lock Bits LB2 and LB1 are programmed to mode 3, EEPROM read does not work from the application code.

Problem Fix/Work around

Do not set Lock Bit Protection Mode 3 when the application code needs to read from EEPROM.

3. **Reading EEPROM at low frequency may not work for frequencies below 900 kHz**

Reading data from the EEPROM at low internal clock frequency may result in wrong data read.

Problem Fix/Workaround

Avoid using the EEPROM at clock frequency below 900kHz.

4. **Timer Counter 1 PWM output generation on OC1B – XOC1B does not work correctly**

Timer Counter1 PWM output OC1B-XOC1B does not work correctly. Only in the case when the control bits, COM1B1 and COM1B0 are in the same mode as COM1A1 and COM1A0, respectively, the OC1B-XOC1B output works correctly.

Problem Fix/Work around

The only workaround is to use same control setting on COM1A(1:0) and COM1B(1:0) control bits, see table 14-4 in the data sheet. The problem has been fixed for Tiny45 rev D.

- **Too high power down power consumption**
- **DebugWIRE loses communication when single stepping into interrupts**
- **PLL not locking**
- **EEPROM read from application code does not work in Lock Bit Mode 3**
- **Reading EEPROM at low frequency may not work for frequencies below 900 kHz**

1. Too high power down power consumption

Three situations will lead to a too high power down power consumption. These are:

- An external clock is selected by fuses, but the I/O PORT is still enabled as an output.
- The EEPROM is read before entering power down.
- VCC is 4.5 volts or higher.

Problem fix / Workaround

- When using external clock, avoid setting the clock pin as Output.
- Do not read the EEPROM if power down power consumption is important.
- Use VCC lower than 4.5 Volts.

2. DebugWIRE loses communication when single stepping into interrupts

When receiving an interrupt during single stepping, debugwire will lose communication.

Problem fix / Workaround

- When singlestepping, disable interrupts.
- When debugging interrupts, use breakpoints within the interrupt routine, and run into the interrupt.

3. PLL not locking

When at frequencies below 6.0 MHz, the PLL will not lock

Problem fix / Workaround

When using the PLL, run at 6.0 MHz or higher.

4. EEPROM read from application code does not work in Lock Bit Mode 3

When the Memory Lock Bits LB2 and LB1 are programmed to mode 3, EEPROM read does not work from the application code.

Problem Fix/Work around

Do not set Lock Bit Protection Mode 3 when the application code needs to read from EEPROM.

5. Reading EEPROM at low frequency may not work for frequencies below 900 kHz

Reading data from the EEPROM at low internal clock frequency may result in wrong data read.

Problem Fix/Workaround

Avoid using the EEPROM at clock frequency below 900kHz.

8.3 Errata ATtiny85

The revision letter in this section refers to the revision of the ATtiny85 device.

8.3.1 Rev B

No known errata.

8.3.2 Rev A

- **Reading EEPROM at low frequency may not work for frequencies below 900 kHz**

1. **Reading EEPROM at low frequency may not work for frequencies below 900 kHz**

Reading data from the EEPROM at low internal clock frequency may result in wrong data read.

Problem Fix/Workaround

Avoid using the EEPROM at clock frequency below 900kHz.

9. Datasheet Revision History

9.1 Rev. 2586J-12/06

1. Updated "Low Power Consumption" on page 1.
2. Updated description of instruction length in "Architectural Overview", starting on page 6.
3. Updated Flash size in "In-System Re-programmable Flash Program Memory" on page 14.
4. Updated cross-references in sections "Atomic Byte Programming", "Erase" and "Write", starting on page 16.
5. Updated "Atomic Byte Programming" on page 16.
6. Updated "Internal PLL for Fast Peripheral Clock Generation - clkPCK" on page 23.
7. Replaced single clocking system figure with two: Figure 7-2 and Figure 7-3 on page 23.
8. Updated Table 7-1 on page 24, Table 7-4 on page 26 and Table 7-6 on page 28.
9. Updated "Calibrated Internal RC Oscillator" on page 27.
10. Updated Table 7-11 on page 29.
11. Updated "OSCCAL – Oscillator Calibration Register" on page 31.
12. Updated "CLKPR – Clock Prescale Register" on page 32.
13. Updated "Power-down Mode" on page 35.
14. Updated "Bit 0" in "PRR – Power Reduction Register" on page 38.
15. Added footnote to Table 9-3 on page 46.
16. Updated Table 12-5 on page 64.
17. Deleted "Bits 7, 2" in "MCUCR – MCU Control Register" on page 65.
18. Updated and moved section "Timer/Counter0 Prescaler and Clock Sources", now located on page 67.
19. Updated "Timer/Counter1 Initialization for Asynchronous Mode" on page 89.
20. Updated bit description in "PLLCSR – PLL Control and Status Register" on page 97 and "PLLCSR – PLL Control and Status Register" on page 107.
21. Added recommended maximum frequency in "Prescaling and Conversion Timing" on page 129.
22. Updated Figure 19-8 on page 134 .
23. Updated "Temperature Measurement" on page 138.
24. Updated Table 19-3 on page 139.

25. Updated bit R/W descriptions in:
 "TIMSK – Timer/Counter Interrupt Mask Register" on page 84,
 "TIFR – Timer/Counter Interrupt Flag Register" on page 84,
 "TIMSK – Timer/Counter Interrupt Mask Register" on page 95,
 "TIFR – Timer/Counter Interrupt Flag Register" on page 96,
 "PLLCSR – PLL Control and Status Register" on page 97,
 "TIMSK – Timer/Counter Interrupt Mask Register" on page 106,
 "TIFR – Timer/Counter Interrupt Flag Register" on page 106,
 "PLLCSR – PLL Control and Status Register" on page 107 and
 "DIDR0 – Digital Input Disable Register 0" on page 143.
26. Added limitation to "Limitations of debugWIRE" on page 145.
27. Updated "DC Characteristics" on page 166.
28. Updated Table 23-4 on page 170.
29. Updated Figure 23-6 on page 173.
30. Updated Table 23-7 on page 173.
31. Updated Table 24-1 on page 179.
32. Updated Table 24-2 on page 179.
33. Updated Table 24-26, Table 24-27 and Table 24-28, starting on page 188.
34. Updated Table 24-29, Table 24-30 and Table 24-31, starting on page 189.
35. Updated Table 24-33 on page 191.
36. Updated Table 24-40, Table 24-41, Table 24-42 and Table 24-43, starting on page 195.

9.2 Rev. 2586I-09/06

1. All Characterization data moved to "Electrical Characteristics" on page 166.
2. All Register Descriptions are gathered up in separate sections in the end of each chapter.
3. Updated Table 13-3 on page 80, Table 13-6 on page 81, Table 13-8 on page 82 and Table 22-4 on page 152.
4. Updated "Calibrated Internal RC Oscillator" on page 27.
5. Updated Note in Table 8-1 on page 34.
6. Updated "System Control and Reset" on page 39.
7. Updated Register Description in "I/O Ports" on page 53.
8. Updated Features in "USI – Universal Serial Interface" on page 111.
9. Updated Code Example in "SPI Master Operation Example" on page 113 and "SPI Slave Operation Example" on page 115.
10. Updated "Analog Comparator Multiplexed Input" on page 123.
11. Updated Figure 19-1 on page 127.
12. Updated "Signature Bytes" on page 153.
13. Updated "Electrical Characteristics" on page 166.

9.3 Rev. 2586H-06/06

1. Updated "Calibrated Internal RC Oscillator" on page 27.
2. Updated Table 7.12.1 on page 31.
3. Added Table 23-1 on page 169.

9.4 Rev. 2586G-05/06

1. Updated "Internal PLL for Fast Peripheral Clock Generation - clkPCK" on page 23.
2. Updated "Default Clock Source" on page 25.
3. Updated "Low-frequency Crystal Oscillator" on page 27.
4. Updated "Calibrated Internal RC Oscillator" on page 27.
5. Updated "Clock Output Buffer" on page 30.
6. Updated "Power Management and Sleep Modes" on page 34.
7. Added "BOD Disable" on page 34.
8. Updated Figure 18-1 on page 123.
9. Updated "Bit 6 – ACBG: Analog Comparator Bandgap Select" on page 124.
10. Added note for Table 19-2 on page 129.
11. Updated "Register Summary" on page 199.

9.5 Rev. 2586F-04/06

1. Updated "Digital Input Enable and Sleep Modes" on page 57.
2. Updated Table 22-15 on page 163.
3. Updated "Ordering Information" on page 203.

9.6 Rev. 2586E-03/06

1. Updated Features in "Analog to Digital Converter" on page 126.
2. Updated Operation in "Analog to Digital Converter" on page 126.
3. Updated Table 19-3 on page 139.
4. Updated Table 19-2 on page 138.
5. Updated "Errata" on page 209.

9.7 Rev. 2586D-02/06

1. Updated Table 7-4 on page 26, Table 7-5 on page 27, Table 7-9 on page 29, Table 7-12 on page 30, Table 7-11 on page 29, Table 10-1 on page 48, Table 19-4 on page 139, Table 22-15 on page 163, Table 23-5 on page 171.
2. Updated "Timer/Counter1 in PWM Mode" on page 89.
3. Updated text "Bit 2 - TOV1: Timer/Counter1 Overflow Flag" on page 96.

4. Updated values in "DC Characteristics" on page 166.
5. Updated "Register Summary" on page 199.
6. Updated "Ordering Information" on page 203.
7. Updated Rev B and C in "Errata ATtiny45" on page 210.
8. All references to power-save mode are removed.
9. Updated Register Addresses.

9.8 Rev. 2586C-06/05

1. Updated "Features" on page 1.
2. Updated Figure 1-1 on page 2.
3. Updated Code Examples on page 17 and page 18.
4. Moved "Temperature Measurement" to Section 19.9 page 138.
5. Updated "Register Summary" on page 199.
6. Updated "Ordering Information" on page 203.

9.9 Rev. 2586B-05/05

1. CLKI added, instances of EEMWE/EEWE renamed EEMPE/EEPE, removed some TBD.
Removed "Preliminary Description" from "Temperature Measurement" on page 138.
2. Updated "Features" on page 1.
3. Updated Figure 1-1 on page 2 and Figure 9-1 on page 39.
4. Updated Table 8-2 on page 38, Table 12-4 on page 64, Table 12-5 on page 64
5. Updated "Serial Programming Instruction set" on page 157.
6. Updated SPH register in "Instruction Set Summary" on page 201.
7. Updated "DC Characteristics" on page 166.
8. Updated "Ordering Information" on page 203.
9. Updated "Errata" on page 209.

9.10 Rev. 2586A-02/05

1. Initial revision.



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